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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,392	10/15/2003	Chen Ou	KYCP0015USA	4444

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/684,392	OU ET AL.
	Examiner	**Art Unit**
	Matthew Landau	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.
2a)☐ This action is **FINAL**.　　2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,27-29,35-39,43 and 51-71* is/are pending in the application.
　4a) Of the above claim(s) *4,5,14,15,21,27,28,57,58,66,67 and 69-71* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-3,6-13,16-20,22,23,29,35-39,43,51-56,59-65 and 68* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *13 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
　a)☐ All b)☐ Some * c)☐ None of:
　　1.☐ Certified copies of the priority documents have been received.
　　2.☐ Certified copies of the priority documents have been received in Application No. _____.
　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
　Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
　Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, Species 6, in the reply filed on March 7, 2005 is acknowledged.

A quick review of the drawings indicates that claims 27 and 28 do not read on the elected species, but instead read on Species 2 and Species 3, respectively. Also, although Applicant indicated claim 38 as withdrawn, it appears that this claim does read on the elected species. It should further be noted that claim 68 should also be considered a linking claim. Therefore, claims 4, 5, 14, 15, 21, 27, 28, 57, 58, 66, 67, and 69-71 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim.

Claim Objections

Claim 38 is objected to because of the following informalities: the limitation "conductive lay" should be changed to "conductive layer ~~lay~~". Also, it is suggested Applicant further amend the claim to clarify the relationship between the second transparent conductive layer and the second electrode. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 10-13, 17-20, 22, 29, 39, 53-56, 59, 63-65, and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Oku et al. (US Pat. 6,051,847, hereinafter Oku).

Regarding claims 1 and 54, Figure 3 of Oku discloses a substrate 31; a first nitride semiconductor stack (33 or 32/33) formed above the substrate, the first nitride semiconductor stack having an epitaxial surface (surface contacting layer 34) and a first rough surface (upper surface exposed and contacting electrode 37), a distance from the epitaxial surface to the substrate being not less than a distance from the rough surface to the substrate; a nitride emitting layer 34 formed on the epitaxial surface; and a second nitride semiconductor stack 35 formed on the nitride emitting layer. It is inherent that the upper surfaces of layer 33 are rough to some degree. Applicant has not defined the term "rough" in terms of how much unevenness a surface must have in order to be considered "rough". Any semiconductor layer is rough on the microscopic level. Note that claims 12 and 13 state that the roughness is between 3nm and 500nm. Therefore, even a surface with a roughness value as low as 3nm can be considered "rough". Regarding claim 54, Oku also discloses a method of forming the above device (col. 18, lines 9-49).

Regarding claims 2 and 55, Figure 3 of Oku discloses the first nitride semiconductor stack 32/33 comprises a nitride buffer layer 32 formed on the substrate 31.

Regarding claims 3 and 56, Figure 3 of Oku discloses a first electrode 37 formed above a first contact area of the first nitride semiconductor stack.

Regarding claims 6 and 59, Figure 3 of Oku discloses a roughness of the first contact area is not greater than a roughness of the first rough surface. Note that the two areas will inherently have the same roughness since they are part of the same surface.

Regarding claims 10 and 63, Figure 3 of Oku discloses the second nitride semiconductor stack 35 as a second rough surface (upper surface). The upper surface of layer 35 is also inherently rough as explained in the rejection of claim 1 above.

Regarding claims 11 and 64, Figure 3 of Oku discloses a second electrode 36 formed above a second contact area of the second nitride semiconductor stack.

Regarding claims 12 and 65, Oku discloses the first rough surface has a roughness of about 7nm (col. 15, lines 1-4).

Regarding claims 13 and 39, Oku discloses the second rough surface has a roughness of 3.2nm (col. 18, lines 47-49).

Regarding claim 17, Oku discloses the substrate 31 is made of sapphire (col. 17, line 66 – col. 18, line 67).

Regarding claims 18-20, Oku discloses the first nitride semiconductor stack 33 comprises GaN, the nitride emitting layer 34 comprises InGaN, and the second nitride semiconductor stack comprises GaN (col. 17, lines 58-61).

Regarding claim 22, Figure 3 of Oku discloses the first nitride semiconductor stack 33 is n-type and the second nitride semiconductor stack 35 is p-type (col. 17, lines 58-61).

Regarding claim 29, Figure 3 of Oku discloses the distance between the first contact area (area of layer 33 below electrode 37) and the substrate 31 is equal to the distance between the first rough surface and the substrate.

Regarding claims 53 and 68, Figure 3 of Oku discloses the second rough surface is an epitaxial surface. Note that the process of making layer 35 is inherently an epitaxial growth process (col. 18, lines 32-41).

Claims 1, 7-10, 16, 35-38, 43, 54, and 60-62 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuo et al. (US PgPub 2002/0096687, hereinafter Kuo).

Regarding claims 1 and 54, Figure 3 of Kuo discloses a substrate 100; a first nitride semiconductor stack 120/130 formed above the substrate, the first nitride semiconductor stack having an epitaxial surface (surface contacting layer 130) and a first rough surface (upper surface exposed and contacting electrode 162), a distance from the epitaxial surface to the substrate being not less than a distance from the rough surface to the substrate; a nitride emitting layer 140 formed on the epitaxial surface; and a second nitride semiconductor stack 132 formed on the nitride emitting layer. It is inherent that the upper surfaces of layer 120 are rough to some degree. Applicant has not defined the term "rough" in terms of how much unevenness a surface must have in order to be considered "rough". Any semiconductor layer is rough on the microscopic level. Note that claims 12 and 13 state that the roughness is between 3nm and 500nm. Therefore, even a surface with a roughness value as low as 3nm can be considered "rough". Regarding claim 54, Kuo also discloses a method of forming the above device (paragraphs [0026] – [0033]).

Regarding claims 7, 8, 60, and 61, Figure 3 of Kuo discloses a reverse tunneling super-lattice contact layer 150 formed on the second nitride semiconductor stack 132, the reverse tunneling contact layer and the second nitride semiconductor stack being formed by opposite types of materials. Note that layer 132 is p-type, and Kuo discloses layer 150 can be n-type (paragraph [0032]).

Regarding claims 9, 16, and 62, Figure 3 of Kuo discloses a second transparent conductive layer (ITO) 160 formed on the reverse tunneling contact layer (paragraph [0033]).

Regarding claim 10, Figure 3 of Kuo discloses the second nitride semiconductor stack 132 has a second rough surface. Note that the upper surface of layer 132 can be considered rough as explained in the rejection of claim 1 above.

Regarding claims 35 and 36, Figure 3 of Kuo discloses a reverse tunneling super-lattice contact layer 150 formed above the second nitride semiconductor stack 132, the reverse tunneling contact layer and the second nitride semiconductor stack being formed by opposite types of materials. Note that layer 132 is p-type, and Kuo discloses layer 150 can be n-type (paragraph [0032]).

Regarding claims 37 and 43, Figure 3 of Kuo discloses a second transparent conductive layer (ITO) 160 formed above the second nitride semiconductor stack 132.

Regarding claim 38, Kuo discloses the transparent electrode 160 can consist of multiple layers (paragraph [0033]). Therefore, it can be considered that the lower layer is the second transparent conductive layer and an upper layer is a second electrode.

Claims 1, 22, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Nitta (US Pat. 5,900,650).

Regarding claim 1, Figure 3 of Nitta discloses Figure 3 of Kuo discloses a substrate 100; a first nitride semiconductor stack 102/103 formed above the substrate, the first nitride semiconductor stack having an epitaxial surface (surface contacting layer 104) and a first rough surface (upper surface exposed and contacting electrode 108), a distance from the epitaxial surface to the substrate being not less than a distance from the rough surface to the substrate; a nitride emitting layer 104 formed on the epitaxial surface; and a second nitride semiconductor stack 105/106 formed on the nitride emitting layer. It is inherent that the upper surfaces of layer 102 are rough to some degree. Applicant has not defined the term "rough" in terms of how much unevenness a surface must have in order to be considered "rough". Any semiconductor layer is rough on the microscopic level. Note that claims 12 and 13 state that the roughness is between 3nm and 500nm. Therefore, even a surface with a roughness value as low as 3nm can be considered "rough".

Regarding claims 22 and 23, Nitta discloses the first nitride semiconductor stack 102/103 is n-type and the second nitride semiconductor stack 105/106 is p-type (col. 4, lines 35-51). Nitta also discloses the conductivity types can be reversed (col. 3, lines 21-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 6, 10, 11, 29, 51, 52, 63, and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heremans et al. (US Pat. 6,504,180, hereinafter Heremans) in view of Nitta.

Regarding claims 1 and 54, Figure 12 of Heremans discloses a substrate 129; a first semiconductor stack (layer directly above dielectric layer 127) having an epitaxial surface (surface contacting layer 10) and a first rough surface 122, a distance from the epitaxial surface to the substrate being not less than a distance from the rough surface to the substrate; an emitting layer 10 formed on the epitaxial surface; and a second semiconductor stack (layers above layer 10) formed on the emitting layer. The difference between Heremans and the claimed invention is the emitting layer and the semiconductor stacks are made of nitride based materials. Figure 3 of Nitta discloses a GaN based light-emitting device, comprising a first nitride semiconductor stack 102/103, a nitride emitting layer 104, and a second nitride semiconductor stack 105/106 (col. 4, lines 35-51). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Heremans by using GaN based semiconductor materials for the purpose of obtaining a light-emitting device that emits light having a shorter wavelength (in the ultraviolet range). Regarding claim 54, Heremans also disclose the method for forming the above device.

Regarding claim 3, Figure 12 of Heremans discloses a first electrode 124 formed above a first contact area of the first semiconductor stack.

Regarding claim 6, Figure 12 of Heremans discloses a roughness of the first contact area is not greater than a roughness of the first rough surface 122.

Regarding claim 10, Figure 12 of Heremans discloses the second semiconductor stack has a second rough surface 41.

Regarding claims 11, Figure 12 of Heremans discloses a second electrode 123 formed above a second contact area of the second semiconductor stack.

Regarding claim 29, Figure 12 of Heremans discloses the distance between the first contact area and the substrate is equal to the distance between the first rough surface and the substrate.

Regarding claims 51 and 52, the product-by-process limitations "wherein the first rough surface and the second rough surface are formed by performing a dry etching process" does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claims 63 and 64, Figure 12 of Heremans discloses forming a second rough surface 41 and a second contact area (area below electrode 123) on the second semiconductor stack.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Matthew C. Landau

Examiner

May 10, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER